A CMOS Power Amplifier With Power Control and T/R Switch for 2.45-GHz Bluetooth/ISM Band Applications

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Abstract – **The design and performance of a 2.45-GHz power amplifier with 3-bit digital power control (30-dB control in 5-dB step) and T/R switch for 2.45-GHz Bluetooth and ISM band applications using 0.18-μm, single-poly six-metal standard CMOS process with thick top-metal (2-μm) and metal-insulator-metal (MIM) capacitor option are presented in this paper. The proposed design uses single-stage Class-AB topology for the power amplifier. In-house extracted models were used for active and passive components to achieve success on silicon for the first time. The power output is +3.5 dBm at 2.45-GHz after the T/R switch. The drain efficiency is 16% including insertion loss of the T/R switch. The circuit operates from a single 1.8V±10% supply and draws total drain current of 8 mA. The operating temperature range is from -40°C to +85°C.**

I. INTRODUCTION

Present day in wireless comunication the band 2.4 – 2.4835 GHz ISM (Industrial, Scientific, and Medical) is becoming popular. The reasons being are Bluetooth, Cordless Phone, Wireless Headphone, toy markets, etc.. Apart from these application related reasons the main reason is the rapid advances in CMOS scaling with which we are able to achieve f_t comparable to bipolar devices. Bluetooth is a technology enabling short-range radio links between portable electronic devices [1]. Low cost, low power consumption and compactness are vital requirements for a Bluetooth transceivers due to its application environment. Use of CMOS technology for transceivers definitely lowers the cost, consumes less power, also ease of power control capability for power amplifier and easy implementation of complete transceiver on a single chip. A CMOS power amplifier promises higher integration as well as lower cost.

The critical and most power hungry block in any RF transmitter is the power amplifier. There are different classes of power amplifiers. Which class to be used when depends mainly on the modulation scheme employed. For Bluetooth the modulation used is GFSK. So, this transmitter does not need high linearity power amplifier.

Fig. 1 gives the general power amplifier topology [2]. The matching network (MN) supplies maximum power to the power transistor M1. The inductor RFC feeds DC power to the drain. The RFC is chosen large enough so that the current through it is substantially constant. The capacitor C1 prevents any DC power dissipation in the load R_L. The tuned tank circuit consisting of L1 and C2 absorbs the transistor's output capacitance and cuts down on out-of-band emissions caused by ever-present non-linearities. It may be mentioned here that even series tuned circuit in place of the parallel tuned circuit can be used to suppress any particular spectral component.

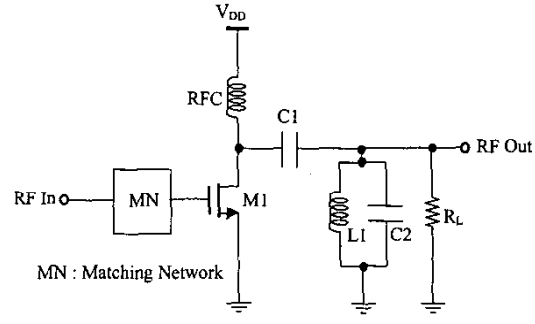

Fig. 1. General power amplifier topology.

The proposed power amplifier with power control and T/R switch is designed for a 0.18-μm CMOS process with a substrate resistivity of 10 Ω-cm. The process has 6 metal layers with thick top metal layer of 2-μm and MIM capacitors. The inductors used are on-chip, realized using only thick top metal layer. Fig. 2 below shows the complete block diagram of the proposed design.

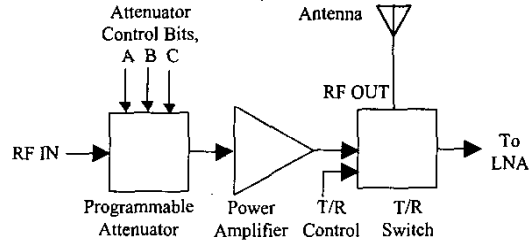

Fig. 2. Block diagram of the proposed power amplifier with power control and T/R switch.

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There are six attenuator steps which are seperated by 5 dB from each other. The topology for power amplifier is single-stage Class-AB. The gate bias for the power amplifier is from PTAT. The T/R switch is nMOS SPDT switch. All the components are on-chip. No external components have been used for the proposed design.

II. CIRCUIT IMPLEMENTATION

Fig. 3 below shows the block diagram of the programmable step attenuator.

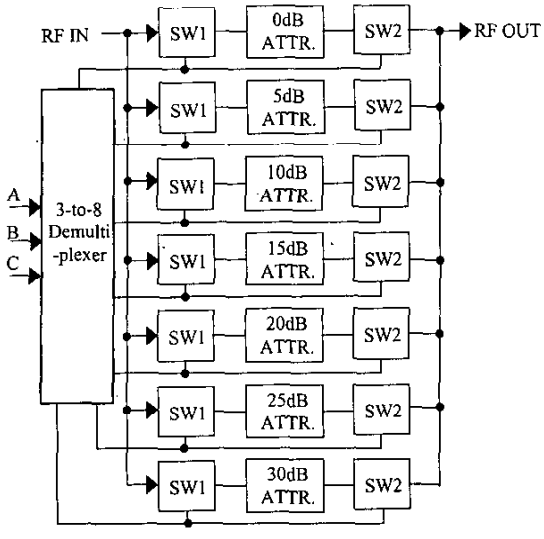


Fig. 3. Block diagram of the programmable attenuator.

The controls for the programmable attenuator are 3-bits (A, B, and C). Only one of the 8 outputs of the 3-to-8 demultiplexer is high for any combination of inputs. SW1 and SW2 use identical transistors. The RF input signal is attenuated by that amount for which the attenuator is selected. Fig. 4 below shows the circuit diagram of the attenuator core.

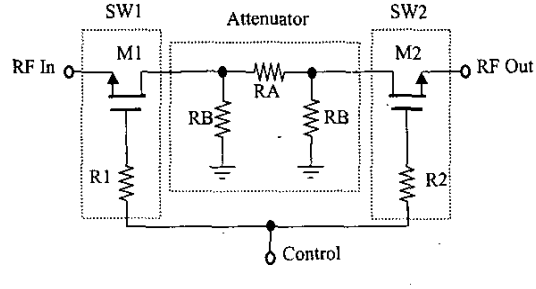


Fig. 4. Schematic of Attenuator Core.

The resistors used for the attenuators are properly laid and also care has been taken in choosing size for the M1 and M2 so that the isolation between input and output is greater than the maximum attenuation step of 30 dB.

The stage following programmable attenuator is the power amplifier. Fig. 5 shows the schematic diagram of the power amplifier [3]. The power amplifier is single-stage class-AB. The capacitor C1, C2 together with L1 constitute high pass input matching circuit. The feedback resistor R1 and capacitor C3 are chosen such that the amplifier is un-conditionally stable. C4, C5 and L3 serves

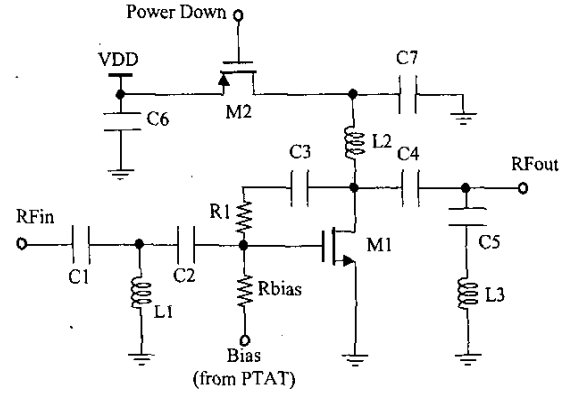


Fig. 5. Schematic of the power amplifier.

as output matching circuit and 2nd harmonic suppressor. The bias for the transistor is from a PTAT circuit. The transistor M2 is power-down switch. The capacitor C7 decouples any leakage of RF power to M2 and to rest of the circuit to ground. The capacitors used are MIM type and all the resistors are poly type. All the inductors are single layer for which thick top metal (2-μm) is used. The inductor and capacitor models are extracted and the same models have been used in the design phase for optimization. Also, in the design phase all the parasitics have been considered. The transmission line models have been considered in the design. The switch transistor M2 used for power down control is large enough to have very very little voltage drop in the power supply voltage.

The schematic diagram of the T/R switch is shown in Fig. 6. The sizes of M1 and M2 are chosen such that the necessary insertion loss and isolation is achieved. Resistors R1 and R2 are large enough so that no RF leaks into buffer or inverter. The resistor R3 provides DC ground. Perfect symmetry is maintained in layout on either side of antenna port.

Detailed measurement results are presented in the next section.

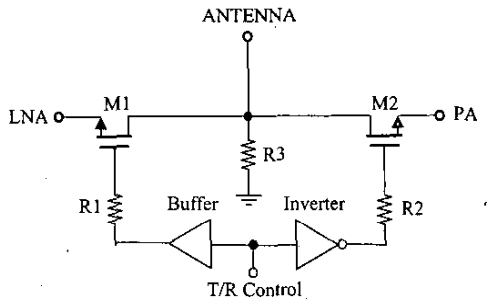


Fig. 6. Schematic of T/R switch.

III. Experimental Results

The proposed IC was fabricated in 0.18-μm standard CMOS process and packaged in a 24-pin QFP package. It takes 0.6-mm^2 silicon area including pads. The die microphotograph is shown in Fig. 7. The device has been evaluated using low-cost 0.8-mm thick dielectric FR4 PCB. The parasitics of the PCB have been de-embedded and the results have been presented in this paper. The extracted package model and printed circuit board parasitics are included in the simulation. The performance of the proposed design exceeds the requirement of class-2 Bluetooth transmitter power.

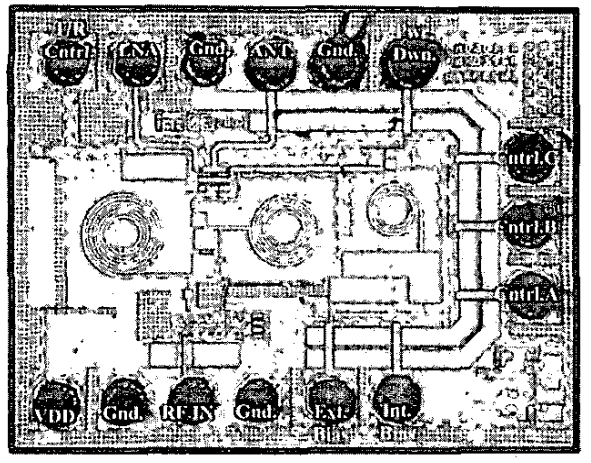


Fig. 7. Microphotograph of the chip.

Table I below shows the measured results. It can be seen that all the Bluetooth specifications are meeting and also this can be used for many applications in 2.45 GHz ISM-band such as cordless phone, wireless headphone.

TABLE I
PERFORMANCE SUMMARY

Parameter	Measured Results
Operating voltage	1.8V±10%
Frequency	2.4 – 2.5 GHz
Power output after T/R switch	+3.5 dBm
2nd and 3rd Harmonic power	<-27 dBm
Isolation	> 40 dB
Power Control	30dB in 5dB step
Current drawn	8 mA
Operating temperature range	-40°C to +85°C

As shown in Fig. 8 the circuits performance has been measured for all the attenuator settings from -40°C to +90°C. The output power variation is within 3dB and the difference between any two consecutive attenuator settings is close to 5dB from -40°C to +90°C. Fig. 9 shows the power output over frequency range 2.25 – 2.65 GHz from -40°C to +90°C. The output power variation in the band 2.4-GHz to 2.5-GHz over the temperature range of -40°C to +90°C is within 3dB.

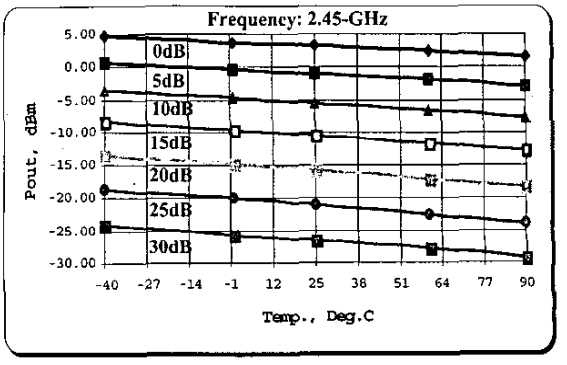


Fig. 8. Power output vs. Temp. for different attenuator setting.

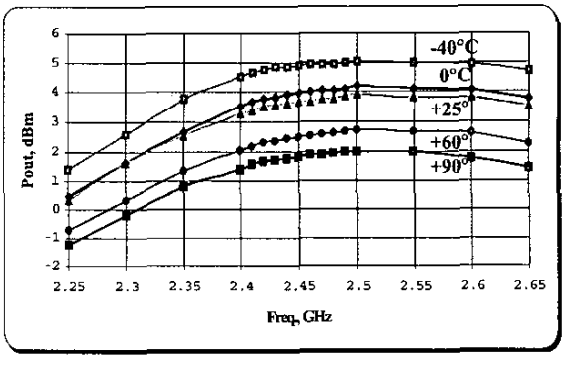


Fig. 9. Power Output vs. Frequency and Temperature.

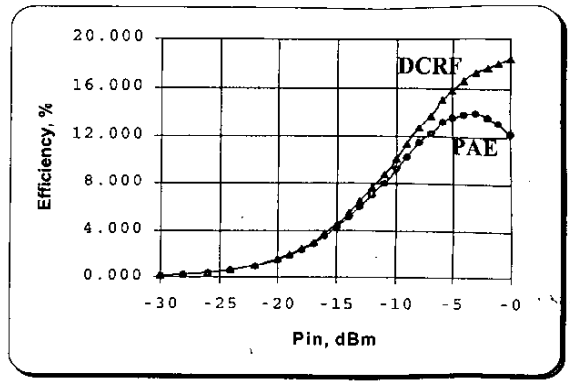


Fig. 10. PAE and DCRF vs. Input Power.

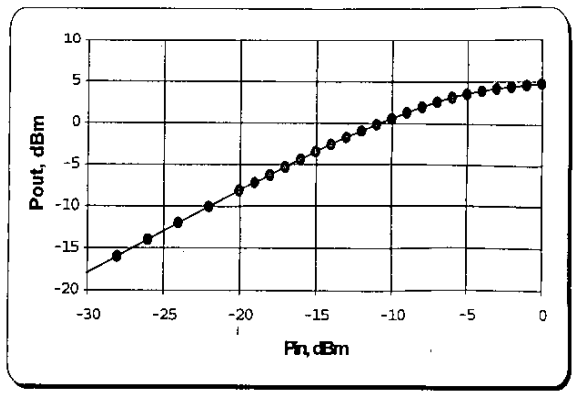
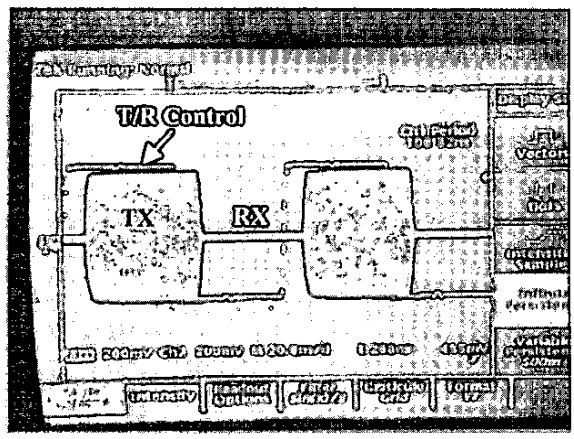


Fig. 11. Input Power vs. Output Power.



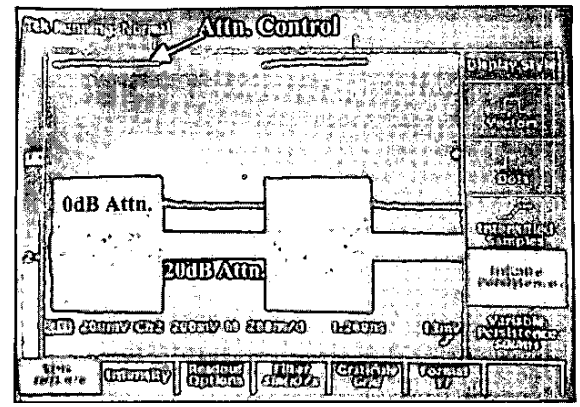


Fig. 13. Programmable Attenuator - Switching waveform for 0 dB and 20 dB attenuator switching.

The power added efficiency (PAE) and DC-RF efficiencies for typical conditions for input power variation from –30 dBm to 0 dBm is given in Fig. 10. Pin vs. Pout plot is shown in Fig. 11. The power amplifier is operated beyond its 1-dB compression point to have very little variation in output power with variation in input power. The switching speed of the T/R switch is very fast as it is shown in Fig. 12. The switching speed is less than 5 nS. The control to the attenuator is switched between 0 dB and 20 dB and output voltage at the antenna port is measured using Tektronix TDS 820 Oscilloscope. The waveform is shown in Fig. 13.

IV. CONCLUSION

The performance of the presented power amplifier with power control and T/R switch exceeds the requirements for the class-2 Bluetooth transmitter. With the use of PTAT biasing for the gate of power transistor the gain variation with temperature has been maintained within 3dB over temperature range -40°C to +90°C.

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REFERENCES

[1] Bluetooth Specifications Version 1.0.
[2] Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits,* Cambridge University Press, 1998.
[3] Ravi Gupta et al., "Design and Optimization of CMOS RF Power Amplifiers," *IEEE Journal of Solid-State Circuits,* Vol.36, No.2, February 2001.